IN THE CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Previously presented) A method of forming a cell area of a flash memory device comprising:

forming an active region having a plurality of line shaped sub-regions on a semiconductor substrate, each being defined parallel to each other by an isolation layer;

forming a gate insulating layer and a silicon floating gate layer in said active region;

forming a floating gate intermediate pattern by patterning said floating gate layer;

forming a dielectric layer over said floating gate intermediate pattern;

forming a silicon control gate layer over said dielectric layer;

forming a plurality of gate lines by partially etching said silicon control gate layer, said dielectric layer, and said floating gate intermediate pattern;

doping said active region between said gate lines by using a dose of impurity below 1.0×10^{15} ions/ cm^2;

forming a lower interlayer insulating layer over the whole surface of said substrate over which said doping is carried out;

forming a groove exposing a common source region in said active region by partially etching said lower interlayer insulating layer;

depositing a silicon layer to fill said groove;

forming a wall shaped silicon common source line and exposing upper portions of said gate lines by planarizing said silicon layer and said lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of said gate lines and on said silicon common source line.

5. (Previously presented) The method of forming a cell area of a flash memory device according to claim 4, further including forming an etch stop layer over said substrate between said doping and said forming said lower interlayer insulating layer.

6. (Previously presented) The method of forming a cell area of a flash memory device according to claim 4,

wherein said forming said groove includes forming first contact holes in bit line contact regions; and

further including:

forming an upper interlayer insulating layer after said forming said metal silicide layer;

forming second contact holes in said bit line regions by partially etching said upper interlayer insulating layer;

depositing a wiring metal layer for bit lines and bit line contacts; and

forming bit lines by patterning said wiring metal layer.

7. (Canceled)

8. (Currently amended) A method of forming a semiconductor device comprising:

forming an active region on a semiconductor substrate, the active region defined by an isolation layer;

sequentially forming a gate insulating layer and a silicon floating gate layer on the active region;

forming a floating gate intermediate pattern by patterning the floating gate layer;

forming an intergate dielectric layer overlying the floating gate intermediate pattern;

forming a silicon control gate layer overlying the intergate dielectric layer;

forming a plurality of gate lines by sequentially patterning the silicon control gate layer, the ~~integrate~~ intergate dielectric layer, and the floating gate intermediate pattern;

forming a lower interlayer insulating layer overlying the plurality of gate lines;

forming a groove to expose a common source region in the active region by etching a portion of the lower interlayer insulating layer;

depositing a silicon layer to fill the groove;

forming a silicon common source line and exposing upper portions of the gate lines by planarizing the silicon layer and the lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of the gate lines and on the silicon common source line.

9. (Previously presented) The method of claim 8, further comprising forming an etch stop layer over the gate lines before forming the lower interlayer insulating layer.